

- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

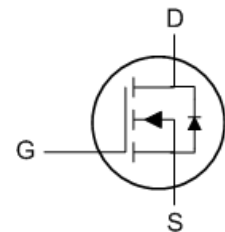
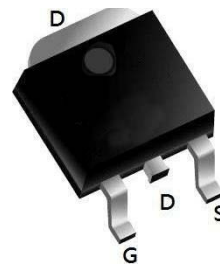

Product Summary

BVDSS	RDSON	ID
60V	6.2mΩ	60A

Description

The XXW60N06 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The XXW60N06 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

TO252-3L Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	60	A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	35	A
I_{DM}	Pulsed Drain Current ²	240	A
EAS	Single Pulse Avalanche Energy ³	280	mJ
I_{AS}	Avalanche Current	---	A
$P_D@T_C=25^{\circ}C$	Total Power Dissipation ⁴	70	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	---	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	2.0	$^{\circ}C/W$

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	---	---	$V/^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=10A$	---	6.2	8	m Ω
		$V_{GS}=4.5V, I_D=5A$	---	---	---	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	3	3.0	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	---	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=60V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=60V, V_{GS}=0V, T_J=100^\circ\text{C}$	---	---	100	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=10A$	15	---	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	---	---	Ω
Q_g	Total Gate Charge	$V_{DS}=50V, V_{GS}=10V, I_D=40A$	---	56	---	nC
Q_{gs}	Gate-Source Charge		---	10	---	
Q_{gd}	Gate-Drain Charge		---	16	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{GS}=10V, V_{DD}=30V,$ $R_G=2.5\Omega, I_D=2A$	---	14.5	---	ns
T_r	Rise Time		---	24	---	
$T_{d(off)}$	Turn-Off Delay Time		---	45	---	
T_f	Fall Time		---	22	---	
C_{iss}	Input Capacitance	$V_{DS}=30V, V_{GS}=0V, f=1\text{MHz}$	---	2873	---	pF
C_{oss}	Output Capacitance		---	252	---	
C_{rss}	Reverse Transfer Capacitance		---	205	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	60	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=10A, T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=10A, di/dt=100A/\mu s,$ $T_J=25^\circ\text{C}$	---	22	---	nS
Q_{rr}	Reverse Recovery Charge		---	27	---	nC

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

3. The EAS data shows Max. rating. The test condition is $V_{DD}=40V, V_{GS}=10V, L=0.5\text{mH}$.

4. The power dissipation is limited by 150°C junction temperature

5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Output Characteristics

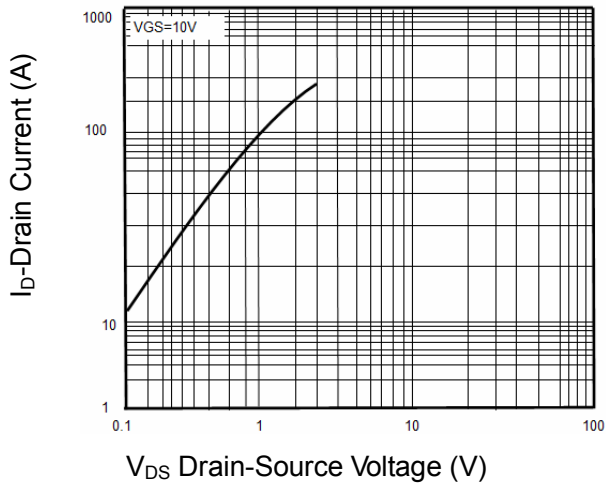


Figure2. Transfer Characteristics

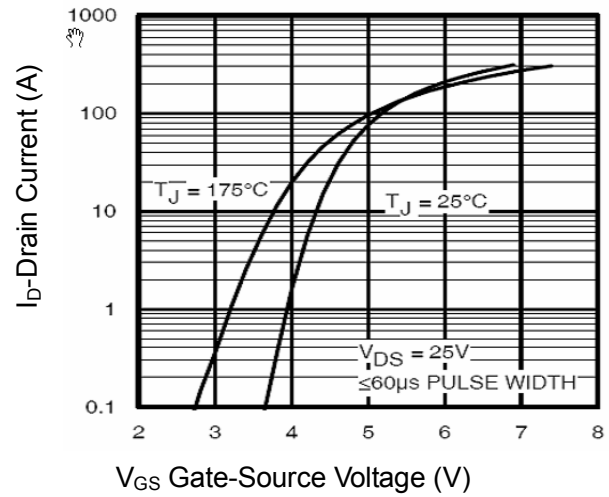


Figure3. BVDSS vs Junction Temperature

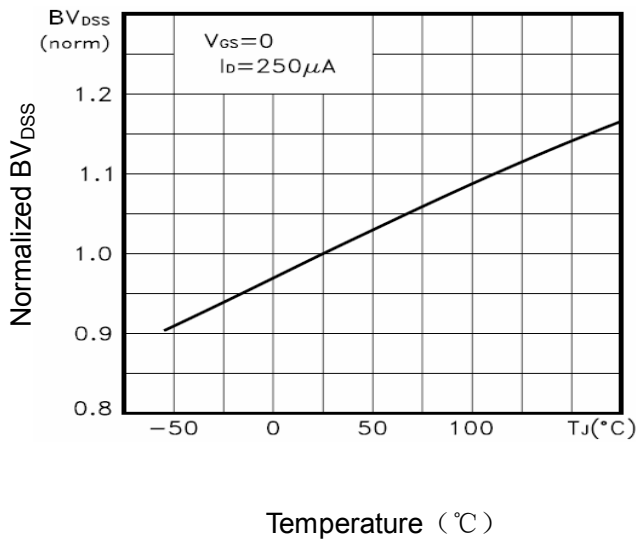


Figure4. ID vs Junction Temperature

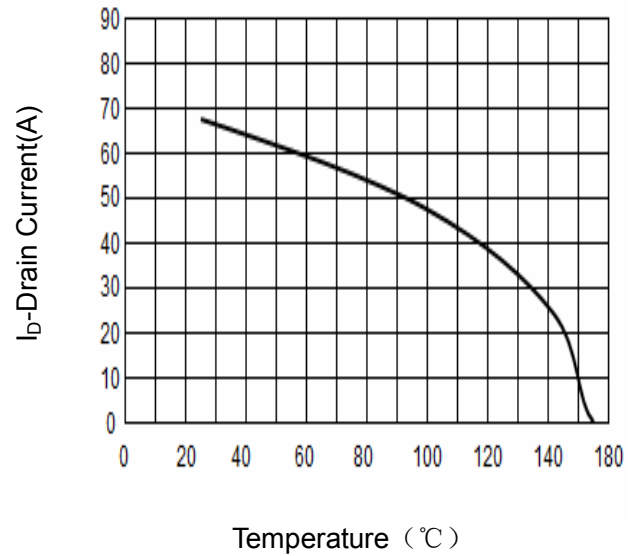


Figure5. VGS(th) vs Junction Temperature

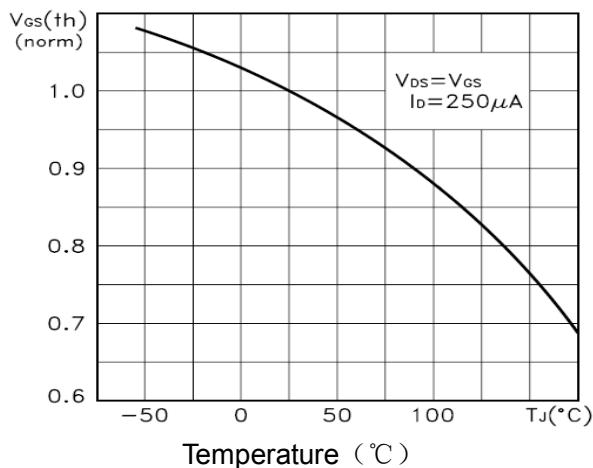


Figure6. Rds(on) Vs Junction Temperature

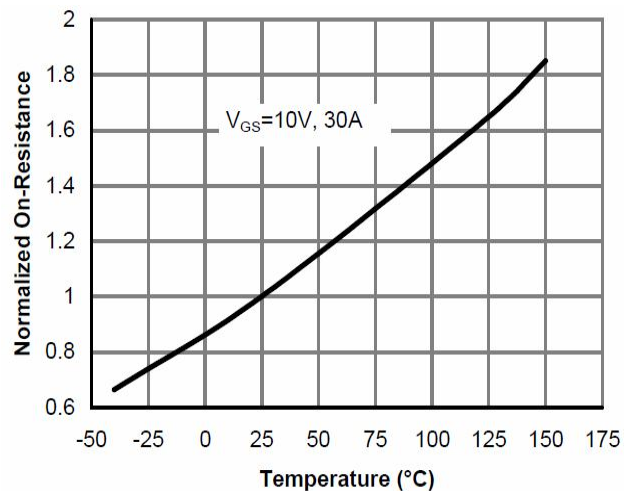


Figure7. Gate Charge

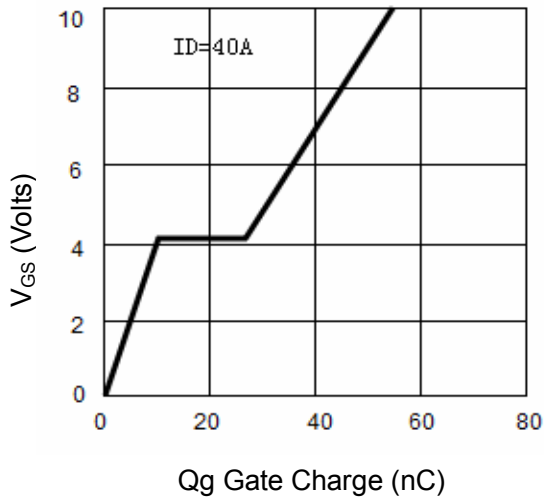


Figure8. Capacitance vs Vds

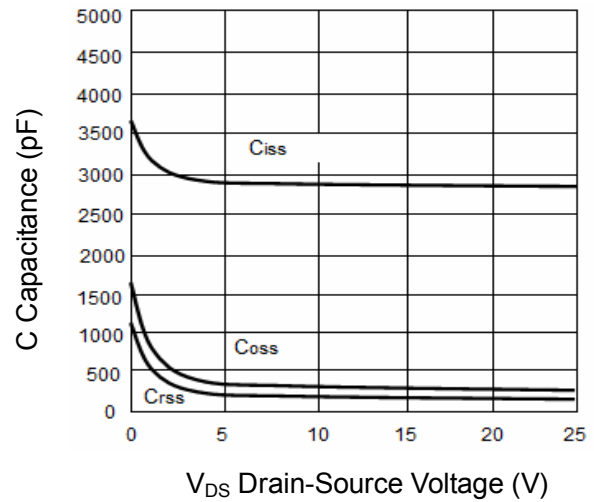


Figure9. Source- Drain Diode Forward

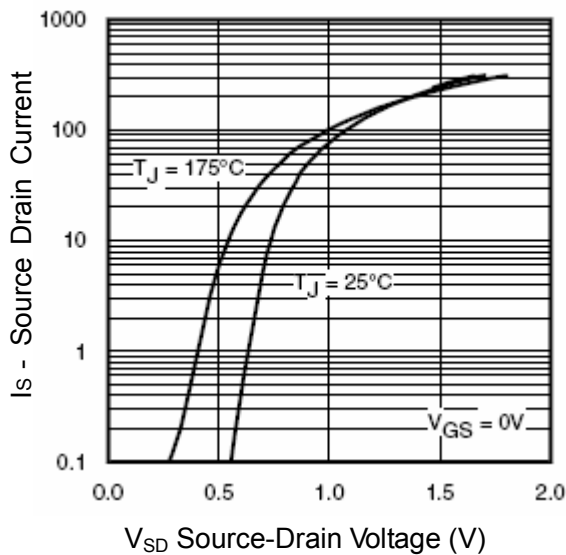


Figure10. Safe Operation Area

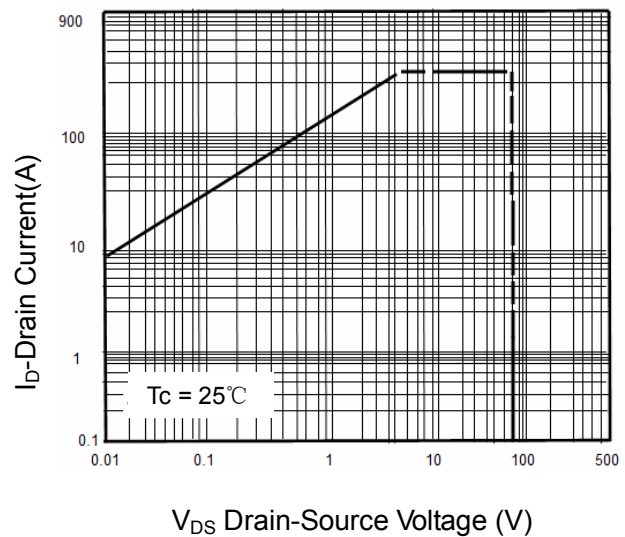
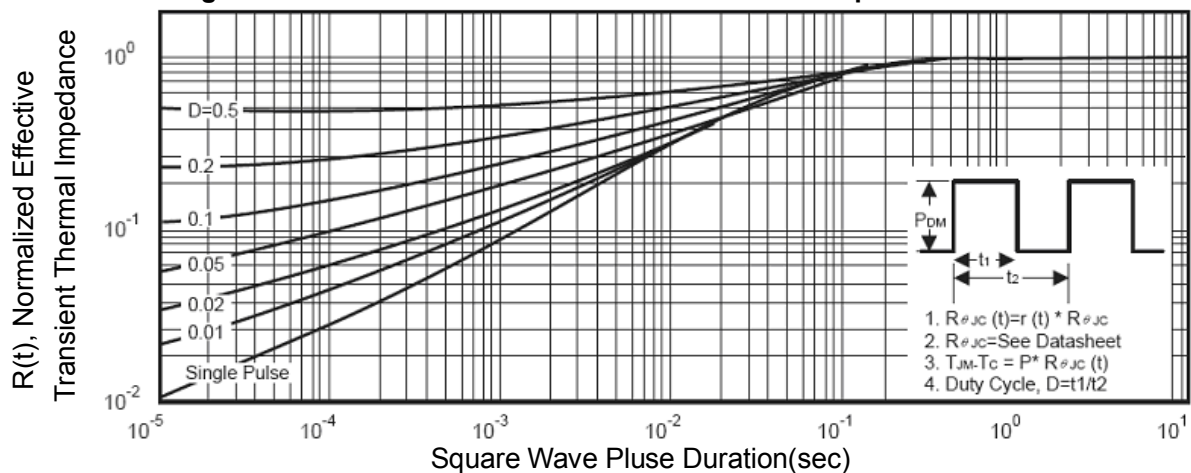
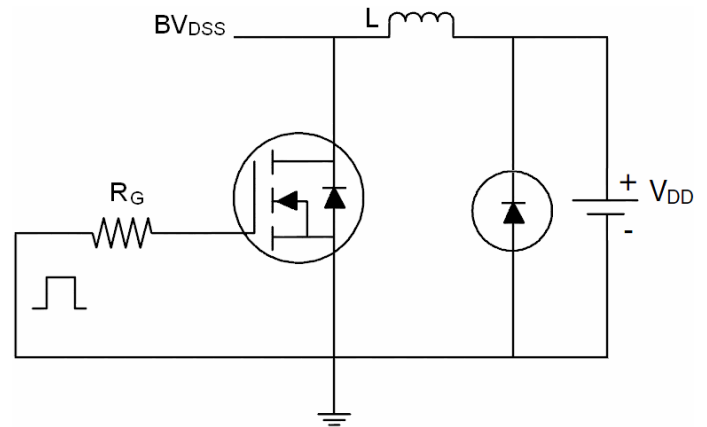
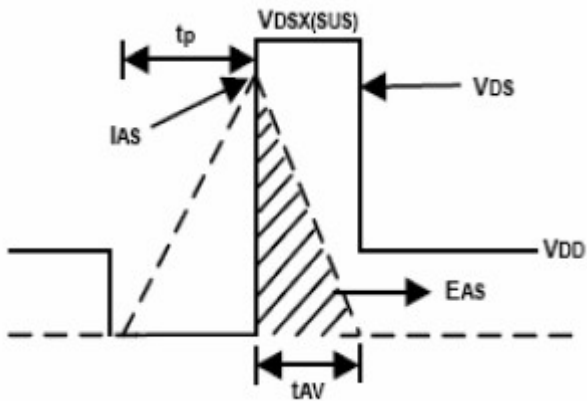


Figure11. Normalized Maximum Transient Thermal Impedance

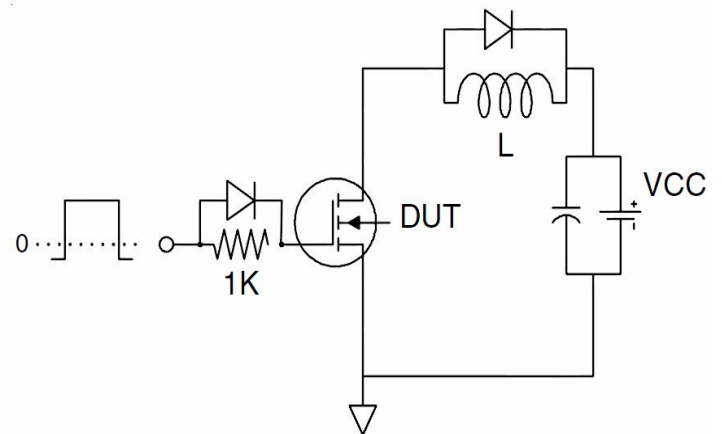
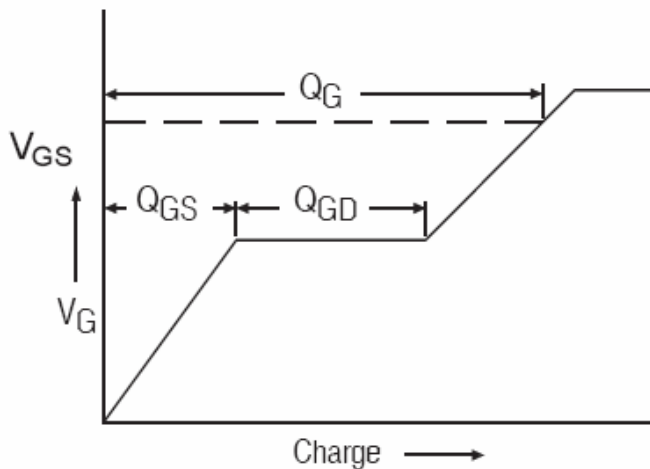


Test Circuit

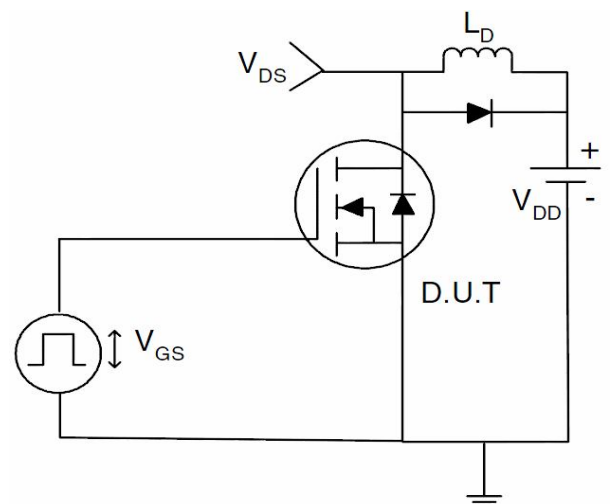
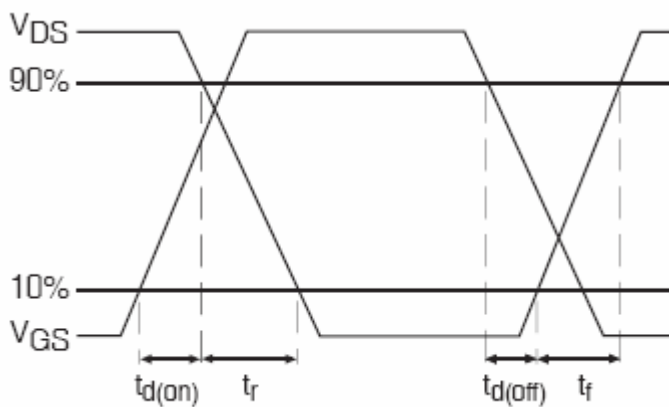
1) E_{AS} Test Circuits



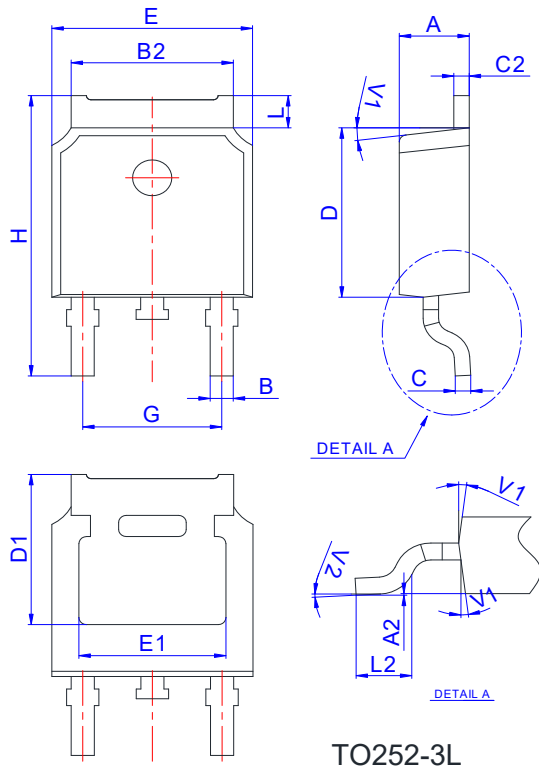
2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:

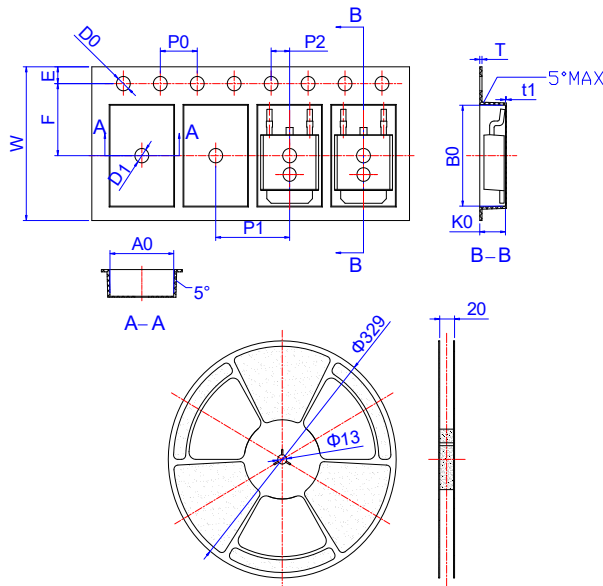


Package Mechanical Data-TO252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583